IN THE CLAIMS

Claims 1-20 are pending in this application. Please amend claims 1, 5-8, 13 and 15-20 as follows:

1. (Currently Amended) A direct conversion receiver comprising:

a pair of mixers which convert a receive signal frequency to a baseband frequency; and

a baseband frequency signal processing block including a pair of first gain control amplifiers and a pair of first filters, following said mixers,

wherein said baseband frequency signal processing block further includes a pair of negative feedback circuits with an adjustable feedback factor, each negative feedback circuit including a second filter of low-pass type.

2. (Original) The direct conversion receiver according to claim 1,

wherein each said negative feedback circuit comprises a second amplifier and said second filter located, following an output end of the second amplifier.

3. (Original) The direct conversion receiver according to claim 2,

wherein said second amplifier is a gain control amplifier.

4. (Original) The direct conversion receiver according to claim 2,

wherein said second filter is a low-pass filter with an adjustable cut-off frequency.

5. (Currently Amended) The direct conversion receiver according to claim 1, further comprising a pair of DC offset cancellation circuits, each comprising:

an analog to digital converter which is connected to an output of one of said pair of first gain control amplifiers to convert analog signals to digital signals;

a digital processing circuit which detects a DC offset voltage out of output signals from said analog to digital converter and calculates a voltage to cancel the DC offset voltage; and

a digital to analog converter which converts a digital signal of the voltage calculated by the digital processing circuit into an analog signal of the voltage and supplies the analog signal of the voltage to said one of said pair of first gain control

amplifiers.

6. (Currently Amended) The direct conversion receiver according to claim 2, further comprising a pair of DC offset cancellation circuits, each comprising:

an analog to digital converter which is connected to an output of one of said pair of first gain control amplifiers to convert analog signals to digital signals;

a digital processing circuit which detects a DC offset voltage out of output signals from said analog to digital converter and calculates a voltage to cancel the DC offset voltage; and

a digital to analog converter which converts a digital signal of the voltage calculated by the digital processing circuit into an analog signal of the voltage and supplies the analog signal of the voltage to said one of said pair of first gain control amplifiers.

7. (Currently Amended) The direct conversion receiver according to claim 3, further comprising a pair of DC offset cancellation circuits, each comprising:

an analog to digital converter which is connected to an output of one of said pair of first gain control amplifiers to convert analog signals to digital signals;

a digital processing circuit which detects a DC offset voltage out of output signals from said analog to digital converter and calculates a voltage to cancel the DC offset voltage; and

a digital to analog converter which converts a digital signal of the voltage calculated by the digital processing circuit into an analog signal of the voltage and supplies the analog signal of the voltage to said one of said pair of first gain control amplifiers.

8. (Currently Amended) The direct conversion receiver according to claim 4, further comprising a pair of DC offset cancellation circuits, each comprising:

an analog to digital converter which is connected to an output of one of said pair of first gain control amplifiers to convert analog signals to digital signals;

a digital processing circuit which detects a DC offset voltage out of output signals from said analog to digital converter and calculates a voltage to cancel the DC offset voltage; and

a digital to analog converter which converts a digital signal of the voltage

calculated by the digital processing circuit into an analog signal of the voltage and supplies the analog signal of the voltage to said one of said pair of first gain control amplifiers.

9. (Original) The direct conversion receiver according to claim 5,

wherein said direct conversion receiver performs DC offset cancellation by means of said pair of DC offset cancellation circuits when being powered on and, subsequently, performs DC offset cancellation by means of said pair of negative feedback circuits.

10. (Original) The direct conversion receiver according to claim 6,

wherein said direct conversion receiver performs DC offset cancellation by means of said pair of DC offset cancellation circuits when being powered on and, subsequently, performs DC offset cancellation by means of said pair of negative feedback circuits.

11. (Original) The direct conversion receiver according to claim 7,

wherein said direct conversion receiver performs DC offset cancellation by means of said pair of DC offset cancellation circuits when being powered on and, subsequently, performs DC offset cancellation by means of said pair of negative feedback circuits.

12. (Original) The direct conversion receiver according to claim 8,

wherein said direct conversion receiver performs DC offset cancellation by means of said pair of DC offset cancellation circuits when being powered on and, subsequently, performs DC offset cancellation by means of said pair of negative feedback circuits.

13. (Currently Amended) The direct conversion receiver according to claim 1,

wherein said pair of first gain control amplifiers have multistage compositions in which a pair of first-stage amplifiers are a pair of static gain amplifiers to which a pair of DC offset cancellation circuits are attached respectively, each said DC offset cancellation circuit comprising:

an analog to digital converter which is connected to an output of one of said

pair of first gain control amplifiers to convert analog signals to digital signals;

a digital processing circuit which detects a DC offset voltage out of output signals from said analog to digital converter and calculates a voltage to cancel the DC offset voltage; and

a digital to analog converter which converts a digital signal of the voltage calculated by the digital processing circuit into an analog signal of the voltage and supplies the analog signal of the voltage to said one of said pair of first gain control amplifiers.

14. (Original) The direct conversion receiver according to claim 13,

wherein said pair of static gain amplifiers perform DC offset cancellation by means of said pair of DC offset cancellation circuits when said direct conversion receiver is powered on and, subsequently, DC offset cancellation is performed by means of said pair of negative feedback circuits.

15. (Currently Amended) The direct conversion receiver according to claim 1,

wherein each of said pair of first gain control amplifiers is made up of multiple stages of gain control amplifiers and a last-stage static gain amplifier and each said negative feedback circuit loops back to an output of a first-stage gain control amplifier.

16. (Currently Amended) The direct conversion receiver according to claim 2,

wherein each of said pair of first gain control amplifiers is made up of multiple stages of gain control amplifiers and a last-stage static gain amplifier and each said negative feedback circuit loops back to an output of a first-stage gain control amplifier.

17. (Currently Amended) The direct conversion receiver according to claim 3,

wherein each of said pair of first gain control amplifiers is made up of multiple stages of gain control amplifiers and a last-stage static gain amplifier and each said negative feedback circuit loops back to an output of a first-stage gain control amplifier.

18. (Currently Amended) The direct conversion receiver according to claim 1,

wherein said pair of first gain control amplifiers are pair of gain control amplifiers having circuitry in which a plurality of different resistance elements are located so as to connect to a common terminal of the emitter side of a couple of differential transistors and gain is changed in steps by switching on/off current flowing through the plurality of resistance elements.

19. (Currently Amended) The direct conversion receiver according to claim 2,

wherein said pair of first gain control amplifiers are pair of gain control amplifiers having circuitry in which a plurality of different resistance elements are located so as to connect to a common terminal of the emitter side of a couple of differential transistors and gain is changed in steps by switching on/off current flowing through the plurality of resistance elements.

20. (Currently Amended) The direct conversion receiver according to claim 3,

wherein said pair of first gain control amplifiers are pair of gain control amplifiers having circuitry in which a plurality of different resistance elements are located so as to connect to a common terminal of the emitter side of a couple of differential transistors and gain is changed in steps by switching on/off current flowing through the plurality of resistance elements.